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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	4307US (99-1193)
First Inventor or Application Identifier	Pary Baluswamy
Title	RESIDUE FREE OVERLAY TARGET
Express Mail Label No.	EL700253658US

09/651190 U.S. PTO 08/30/00

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [ ] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 15] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 10]
4. Oath or Declaration [Total Pages 2]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
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   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [X] Other: Unexecuted Declaration

** A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.*

17. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
    [ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
    Prior application information: Examiner _____ Group / Art Unit: _____

18. CORRESPONDENCE ADDRESS

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Signature	Samuel Webb	Date	08/30/00

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Attorney Docket 4307US (99-1193)

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APPLICATION FOR LETTERS PATENT

for

RESIDUE FREE OVERLAY TARGET

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RESIDUE-FREE OVERLAY TARGET

BACKGROUND OF THE INVENTION

Field of the Invention: The present invention relates to the field of semiconductor device fabrication. Specifically, the present invention provides a residue-free overlay target which enables precise alignment of lithographic masks or reticles while substantially preventing residue build up at the surface of the semiconductor substrate and eliminating process steps associated with known overlay targets.

State of the Art: As is well known, state of the art semiconductor memory and processing devices include multiple layers of electronic features which must be fabricated using multiple process steps. Individual features of state of the art semiconductor devices are generally defined by photolithograpic processes wherein a resist is applied over the surface of a semiconductor substrate, or a material layer overlying a semiconductor substrate, and individual device features are patterned into the resist using a mask or reticle. After patterning the resist, the device features are permanently defined in the material layer being processed or the underlying semiconductor substrate by wet or dry etch steps. Advanced processes used to fabricate state of the art semiconductor devices may require as many as fifteen or more separate patterning and etching steps at varying layers during the fabrication process. However, in order to consistently fabricate functional and reliable semiconductor devices, it is necessary that each pattern be accurately aligned over the semiconductor substrate or material layer being processed, and the feature dimensions must be precisely defined at each patterning and etch step. This is particularly true for state of the art semiconductor devices, which require tolerances in the tens of nanometers range.

To help ensure that the device patterns are accurately positioned, a mask or reticle may be aligned using overlay targets located outside the chip pattern defined on the wafer being processed. Overlay targets are generally etched into the semiconductor substrate or into an overlying material layer and, therefore, become a permanent part of the wafer being processed. As new layers are deposited, patterned, and etched, the new masks or reticles used to process the new layers are often aligned by referencing back to the permanent overlay targets previously defined in an underlying material layer.

Manual or automated registration tools may be used for pattern alignment, which is generally accomplished by aligning overlay targets with marks included on the mask or reticle

used. In state of the art fabrication facilities, however, automated registration tools are preferred because of their accuracy and high throughput capabilities. To accomplish their task, such automated registration tools must be able to readily detect the edges of the pattern formed by the overlay targets. Yet, as will be described hereinafter, known overlay targets enable intermittent accumulation of process residue which obscures the edges of the overlay target patterns, thereby substantially interfering with the proper function of registration tools.

Known overlay targets generally include a pattern formed by one or more etched trenches or pad areas. Illustrated in drawing FIG. 1 is a portion of an intermediate wafer structure 5 including a simple trench-type overlay target 10. The overlay target 10 includes a continuous rectangular trench 12 etched into the semiconductor substrate 14 outside the chip pattern 16. Of course, the overlay target depicted in drawing FIG. 1 is provided for illustrative purposes only. It is understood that overlay targets can be created using a variety patterns formed from continuous trenches, discontinuous trenches, or pad areas.

Depicted in drawing FIG. 2 is a cross section taken at line A-A of drawing FIG. 1 and illustrates an overlying material layer 16 deposited over the surface 18 of the semiconductor substrate 14 after formation of the trench 11 defining the overlay target. As can be seen in drawing FIG. 2., the overlying material layer 16 tends to conform to the topography created by the trench 11. Such conformation results in the formation of depressions 20 at the upper surface 22 of the overlying material layer 16. Even after a polishing step, portions 24 (shown in drawing FIG. 3) of the depressions 20 may still remain and serve as collection points for process residue 26, such as hemispherical grain ("HSG") Poly. As is shown in drawing FIG. 4, because the residue 26 overlies the trench 11 defining overlay target, the residue 26 works to obscure the outlines (depicted by dashed lines 28a and 28b) of the pattern formed by the trench 11, making the outlines 28a, 28b appear ragged or inconsistent. Though drawing FIG. 2 through drawing FIG. 4 depict features associated with a trench-type overlay target, intermittent collection of obscuring residue is also an issue pad-type overlay targets and overlay targets including one or more trenches or pads.

Though the build up of process residue over an overlay target may occur only intermittently across the surface of a wafer, even one obscured overlay target may render mask or reticle alignment impossible or, at best, imprecise. For this reason, the surface of an incomplete

wafer must be periodically cleaned, such as, for example, by patterning and etching steps, in order to ensure each of the overlay targets formed in the wafer are clean and easily registered by a registration tool. As is easily appreciated, such cleaning steps add time and cost to the fabrication process. Therefore, a overlay target which does not lead to the collection of obscuring process residue would be an improvement in the art, obviating the cost and delay associated with the cleaning steps currently undertaken to ensure the proper registration of overlay targets.

SUMMARY OF THE INVENTION

The present invention includes a residue-free overlay target, as well as a method of forming a residue-residue free overlay target, which answer the foregoing needs. The trenches or pads forming the residue-free overlay target of the present invention are broken down into a series of smaller raised lines which substantially eliminate any surface topography, such as depressions, at the top surface of overlying material layers. The residue-free overlay target of the present invention, therefore, prevents the formation of surface features which could serve as collection points for obscuring process residue, thereby eliminating the need to perform the intermediate cleaning steps otherwise necessary to ensure registration of overlay targets.

The method of forming a residue-free overlay target of the present invention may be accomplished and modified using process technology known in the semiconductor fabrication art. The method of the present invention includes providing a semiconductor substrate having top and bottom surfaces, depositing a resist layer, exposing the resist layer using a mask or reticle creating a resist pattern corresponding to at least one overlay target according to the present invention, developing said resist pattern, and executing a wet or dry etch to create at least one overlay target including a trench or pad area including a series of raised lines. As will be understood by those of skill in the art, the method of the present invention may be used to create overlay targets having a variety of patterns suitable for different semiconductor device fabrication processes, as well as different manual or automated registration tools. Moreover, the method of the present invention is easily modified for the fabrication of overlay targets in a variety of substrates.

Other features and advantages of the present invention will become apparent to those of skill in the art through a consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The Figures presented in conjunction with this description are not actual views of any particular portion of an actual semiconducting device or component, but are merely representations employed to more clearly and fully depict the present invention.

FIG. 1 provides a top view of a portion of a semiconductor wafer including an overlay target and a portion of the chip pattern formed on the semiconductor wafer;

FIG. 2 depicts a cross section of a portion of the structure illustrated in FIG. 1, the cross section being taken at line A-A of FIG. 1 and after an additional material layer is formed over the overlay target;

FIG. 3 depicts the same structure as shown in FIG. 2 after the additional material layer has undergone a polishing process;

FIG. 4 provides a top view of the same portion of a semiconductor wafer as is depicted in FIG. 1 after an additional material layer has been deposited over the overlay target and the additional material layer has been subjected to a polishing step;

FIG. 5 provides a top view of a portion semiconductor wafer having an overlay target according to a first embodiment of the overlay target of the present invention formed thereon;

FIG. 6 depicts a cross section of a portion of the structure illustrated in FIG. 5, the cross section being taken at line B-B of FIG. 5;

FIG. 7 provides a top view of a portion semiconductor wafer having an overlay target according to a second embodiment of the overlay target of the present invention formed thereon;

FIG. 8 depicts a cross section of a portion of the structure illustrated in FIG. 7, the cross section being taken at line C-C of FIG. 7;

FIG. 9 provides a top view of a portion semiconductor wafer having an overlay target according to a third embodiment of the overlay target of the present invention formed thereon;

FIG. 10 depicts a cross section of a portion of the structure illustrated in FIG. 9, the cross section being taken at line D-D of FIG. 9;

FIG. 11 depicts a cross section of the same structure illustrated in FIG. 6 after an additional material layer has been deposited over the semiconductor wafer;

FIG. 12 is a micrograph showing a top view of a prior art overlay target obscured by accumulated process residue;

FIG. 13 is a micrograph taken at higher magnification showing the same top view of the overlay target depicted in FIG. 12 after the semiconductor wafer has been subjected to a cleaning process;

FIG. 14 is a micrograph showing a top view of an overlay target according to the present invention;

FIG. 15 - FIG. 18 illustrate various structures at different steps of a method according to the first embodiment of the method of the present invention; and

FIG. 19 - FIG. 22 illustrate various structures at different steps of a method according to the second embodiment of the method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention includes a residue-free overlay target useful in the fabrication of state of the art semiconductor devices. The overlay target of the present invention includes one or more trenches or pad areas including a series of raised lines which substantially prevent subsequently deposited material layers from conforming to the topography of the overlay target. Because the subsequently deposited material layers do not conform to the overlay target topography, the overlay target of the present invention prevents formation of surface topography which could serve to collect obscuring process. Thus, the overlay target of the present invention simplifies current fabrication methods by eliminating the cleaning steps otherwise necessary to remove accumulated process residue and ensure registration of overlay targets after deposition and processing of subsequently applied material layers.

In a first embodiment, illustrated in drawing FIG. 5, the overlay target 30 of the present invention includes a continuous trench 32 having a plurality of raised lines or substantially vertically extending ribs or protrusions 34 disposed therein or from the bottom of the trench thereof. As can be seen in drawing FIG. 6, a cross section of the overlay target 30 taken at line B-B of drawing FIG. 5, the raised lines 34 disposed within the continuous trench 32 originate at the bottom surface 36 of the continuous trench 32 and are defined by alternating spaces 38 etched into surface 39 of a first material layer 40 deposited over the semiconductor wafer 42. Although, drawing FIG. 5 and drawing FIG. 6 illustrate an overlay target 30 including only a single continuous trench 32 forming a generally rectangular pattern, it should be understood that one or

more continuous trenches may be used to form an overlay target of the present invention and that such trenches may be configured in a variety of shapes or sizes to meet any particular processing need.

In another embodiment, illustrated in drawing FIG. 7, the overlay target 30 includes a plurality of discontinuous trenches 44 creating a pattern that can be evaluated by a registration tool. The discontinuous trenches 44 of the second embodiment each include a series of raised lines 34, and as can be clearly seen in drawing FIG. 8, a cross section taken at line C-C of drawing FIG. 7, the raised lines 34 originate from the bottom surfaces 46 of each discontinuous trench 44 and are defined by alternating spaces 38 etched into the surface 39 of a first material layer 40 deposited over the semiconductor wafer 42. Although the discontinuous trenches 44 of the overlay target 30 illustrated in drawing FIG. 7 form a generally rectangular outline, it should be understood that the overlay target of the present invention may also include a plurality of discontinuous trenches disposed in any other pattern suitable for a particular fabrication process or registration tool.

A third embodiment of the overlay target 30 of the present invention is illustrated in drawing FIG. 9. The third embodiment of the overlay target of the present invention is similar to the previous two embodiments except that instead of continuous or discontinuous trenches, the overlay target 30 of the third embodiment includes a pad area 48 including a plurality of raised lines 34 defined by a plurality of alternating spaces 38 etched into the surface 39 of a first material layer 40 deposited over a semiconductor wafer 42 (shown in drawing FIG. 10, a cross section taken at line D-D of drawing FIG. 9). As can be seen in drawing FIG. 10, the raised lines 34 within the pad area 48 originate at the bottom surface 50 of the pad area 48.

It is significant to note that even though the three preceding embodiments of the overlay target of the present invention include either one or more continuous trenches, a plurality of discontinuous trenches, or a pad area, the overlay target of the present invention is not so limited. The overlay target of the present invention may include more than one pad area, one or more continuous trenches in combination with one or more discontinuous trenches, one or more pad areas in combination with one or more continuous trenches and one or more discontinuous trenches, or one or more pad areas in combination with one or more continuous trenches or one or more discontinuous trenches. As will be understood by one of skill in the art, any combination of

continuous trenches, discontinuous trenches, or pad areas may be used, provided that each trench or pad area includes a series of spaced, raised lines and each overlay target forms a pattern that can be evaluated by a registration tool.

The spaced raised lines included in each of the trenches or pad areas of an overlay target of the present invention substantially prevent overlying material layers from conforming to the topography of the overlay target. Illustrated in drawing FIG. 11 is the same cross section of material illustrated in drawing FIG. 6 after a second material layer 52 has been deposited over the surface 39 of the first material layer 40, which has been etched to include the overlay target 30. The spaces 38 defining the raised lines 34 of the overlay target of the present invention are sufficiently narrow that the second material layer 52 does not substantially conform to the topography of the overlay target 30. As a result, the topography of the overlay target 30 is not transferred to the second material layer, and the top surface 54 of the second material layer 52 does not include depressions which collect process residue in sufficient quantities to interfere with the operation of a registration tool. Therefore, the raised lines of the overlay target of the present invention eliminates periodic cleaning steps which would otherwise be necessary to ensure the overlay targets may be accurately evaluated by a registration tool.

Additionally, the spaces defining the raised lines included in each of the trenches or pad areas of an overlay target of the present invention may be of various widths. For example, the widths of the spaces defining the raised lines may be increased where a less conforming material is deposited over the overlay target, or the widths of the spaces defining the raised lines may be decreased where a highly conforming material is deposited over the overlay target. Moreover, the widths of the spaces defining the raised lines included in the overlay target of the present invention may be varied depending on the capabilities of the registration tool used.

Although drawing FIG. 5 through drawing FIG. 11 depict overlay targets etched into the first material layer applied over a semiconductor wafer, it should be understood that the overlay target may also be etched directly into the surface of the semiconductor substrate. Alternatively, as two or more sets of overlay targets are generally used to complete fabrication of state of the art semiconductor devices, an overlay target according to the present invention may also be created in material layers deposited after a first material layer has been deposited and processed as needed.

A useful comparison is illustrated in drawing FIG. 12, FIG. 13 and FIG. 14 showing the desirability of an overlay target according to the present invention. Provided in drawing FIG. 12 is a micrograph of a top view of a trench-type overlay target as seen through a subsequently applied material layer. The continuous trench forming the overlay target of drawing FIG. 12 lacks the raised lines of the overlay target of the present invention, and, therefore, the topography of the trench has transferred to the top surface of the subsequently applied material layer, resulting in a depression in the top surface of the subsequently applied material layer corresponding to the trench forming the overlay target. As can be seen in drawing FIG. 12, during a polishing step, process residue, HSG Poly in this case, has collected in the depression corresponding to the overlay target trench, and the outline of the overlay target appears ragged and inconsistent.

To ensure that the overlay target shown in drawing FIG. 12 is properly read, the semiconductor wafer must be subjected to a cleaning process. For example, the semiconductor wafer may be cleaned by depositing a layer of resist over the semiconductor wafer, exposing and developing the resist to create a photoresist mask exposing the area(s) to be cleaned, etching the exposed area(s) of the semiconductor wafer, and stripping the photoresist mask after the etching process is complete. FIG. 13 provides a second micrograph at higher magnification of a top view of the trench shown in drawing FIG. 12 after the semiconductor wafer has been cleaned by such a process, and, as is easily ascertainable from drawing FIG. 13, the outlines of the overlay target are clearly discernible through the overlying material layer after the cleaning process. But the need to clean the surface of the wafer being processed adds several process steps that increase fabrication cost and decrease throughput.

Provided in drawing FIG. 14 is a micrograph of a top view of an overlay target of the present invention as seen through an overlying material layer. As was the case with the structure depicted in drawing FIG. 12, the overlying material layer of the structure pictured in drawing FIG. 14 has been subjected to a polishing step. However, because the raised lines (not discernible in drawing FIG. 14) included in the trenches of the overlay target shown in drawing FIG. 14 prevent the overlying layer from conforming to the topography of the overlay target, the top surface of the overlying material layer does not include depressions that collect process residue, and, as a result, no process residue obscures the features of the overlay target depicted in drawing FIG. 14. Therefore, the overlay target of the present invention is easily evaluated by registration machinery

without additional cleaning steps, such as those described in relation to drawing FIG. 13, resulting in advantageous cost savings as well as an increase in throughput.

The present invention also includes a method for forming an overlay target, which will be described in relation to drawing FIG. 15 through drawing FIG. 22. A first embodiment of the method of the present invention includes providing a semiconductor substrate 60 having top surface 62 and a bottom surface 64. The semiconductor substrate 60 may be made from any suitable material, such as silicon, gallium, or sapphire materials, and the semiconductor substrate 60 may include one or more doped regions. A material layer 66, such as a borophosphosilicate glass layer or other dielectric, is then deposited over the top surface 62, and a layer of resist 68 is deposited over the material layer 66. The layer of resist 68 may include any suitable resist known in the art, and the resist layer may be applied by any known means, such as, for example, known spin coating processes. As shown in drawing FIG. 16, the layer of resist 68 is then exposed and developed as is known in the art to provide a resist pattern 70 that will result in a desired overlay target. The material layer 66 deposited over the top surface 62 of the semiconductor wafer 60 is then etched, such as, for example, by an NF_3 or a chlorine etch, providing an overlay target 72 of the present invention including a plurality of raised lines 74, as can be seen in drawing FIG. 17 and drawing FIG. 18, a cross section taken at line E-E of drawing FIG. 17.

Though this first embodiment of the method of the present invention has been illustrated using a first material layer as the layer in which the overlay target is fabricated, the first embodiment of the method of the present invention is not so limited. The material layer used for creation of the overlay target need not be the first material layer deposited over the semiconductor substrate. The method according to the first embodiment may also be used to produce overlay targets in any material layer overlying the semiconductor substrate.

In a second embodiment of the method of the present invention the overlay target is etched directly into the semiconductor substrate 60. Thus, as is shown in drawing FIG. 19, the method according to the second embodiment requires providing a semiconductor substrate 60 having a top surface 62 and a bottom surface 64 and depositing a resist layer 68 over the top surface 62 of the semiconductor substrate 60. Again the semiconductor substrate 60 may constitute any suitable semiconductor material, such as those described in relation to the first embodiment. Further, any suitable resist, such as those already described, may be used, and the resist layer 68 may be

deposited by any appropriate method for the resist material used, such as, for example, spinning. After the resist layer 68 is deposited, the resist layer 68 is exposed and developed as is known in the art to form a resist pattern 70 (shown in drawing FIG. 20) that will result in a desired overlay target after etching. The semiconductor substrate 60 is then etched by any known process suitable for the material used to form the semiconductor substrate 60, such as, for example, an NF_3 or a chlorine etch. As can be seen in drawing FIG. 21 and drawing FIG. 22, a cross section of drawing FIG. 21 taken at line F-F, etching the semiconductor substrate 60 provides an overlay target 72 according to the present invention including a plurality of raised lines 74.

It will be easily understood by one of ordinary skill in the art that the method of the present invention is extremely flexible. The method of the present invention is easily adapted to create overlay targets in a variety of substrates using known patterning and etching processes. Moreover, the method of fabricating an overlay target of the present invention may be used to fabricate overlay targets comprising virtually any suitable target pattern.

Though the overlay targets and method of the present invention have been described herein with reference to specific examples, such examples are for illustrative purposes only. The scope of the present invention is defined by the appended claims and is, therefore, not limited by the preceding description and drawings

CLAIMS

What is claimed is:

1. An overlay target comprising:

at least one trench including a series of raised lines.

2. The overlay target of claim 1, wherein said at least one trench comprises a continuous trench defining a geometric shape.

3. The overlay target of claim 1, wherein said at least one trench comprises a plurality of trenches defining said overlay target, each of said plurality of trenches including a series of raised lines.

4. The overlay target of claim 3, wherein said plurality of trenches includes at least one continuous trench defining a geometric shape.

5. An overlay target comprising:

at least one pad area including a series of raised lines.

6. The overlay target of claim 6, wherein said at least one pad area includes a plurality of pad areas defining said overlay target, each of said pad areas including a series of raised lines.

7. The overlay target of claim 6, further comprising at least one trench including a series of raised lines.

8. A semiconductor wafer comprising:

a semiconductor substrate; and

an overlay target comprising at least one series of raised lines.

9. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into said semiconductor substrate.

10. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is etched into a material layer overlying said semiconductor substrate.

11. The semiconductor wafer of claim 8, wherein said at least one series of raised lines of is disposed in at least one trench.

12. The semiconductor wafer of claim 11, wherein a plurality of trenches and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of trenches including one of said plurality of series raised lines.

13. The semiconductor wafer of claim 8, wherein said at least one series of raised lines is disposed in at least one pad area.

14. The semiconductor wafer of claim 13, wherein a plurality of pad areas and a corresponding plurality of series of raised lines define said overlay target, each of said plurality of pad areas including one of said plurality of series of raised lines.

15. The semiconductor wafer of claims 8, wherein said at least one series of raised lines comprises a first series of raised lines disposed in a pad area and a second series of raised lines disposed in a trench.

16. A method for forming an overlay target including a series of raised lines, the method comprising:

providing a substrate;

depositing a resist layer over said substrate;

patterning said resist layer to include a pattern defining said overlay target including a series of raised lines; and

etching said substrate to form said overlay target including a series of raised lines.

17. The method of claim 16, wherein providing a substrate comprises providing a semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates.

18. The method of claim 17, wherein depositing a resist layer over said substrate comprises depositing a resist layer directly over said semiconductor substrate selected from the group consisting of silicon, gallium, and sapphire substrates

19. The method of claim 16, wherein providing a substrate includes providing a semiconductor substrate having a top surface, a bottom surface, and a material layer deposited over said top surface.

20. The method of claim 19, wherein depositing a resist layer over said substrate comprises depositing a resist layer over said material layer and said etching said substrate to form said overlay target comprises etching said material layer.

ABSTRACT OF THE DISCLOSURE

The present invention includes a residue-free overlay target, as well as a method of forming a residue-residue free overlay target. The residue-free overlay target of the present invention is defined by trenches or pads including a series of raised lines. The raised lines included in the overlay target of the present invention substantially eliminate any surface topography, such as depressions, at the top surface of overlying material layers, and, thereby, prevent accumulation of process residue which may obscure the overlay target and inhibit further processing. The method of the present invention may be accomplished and modified using process technology known in the semiconductor fabrication art and includes providing a semiconductor substrate, depositing a resist layer, patterning the resist, and executing a wet or dry etch to create at least one overlay target according to the present invention.

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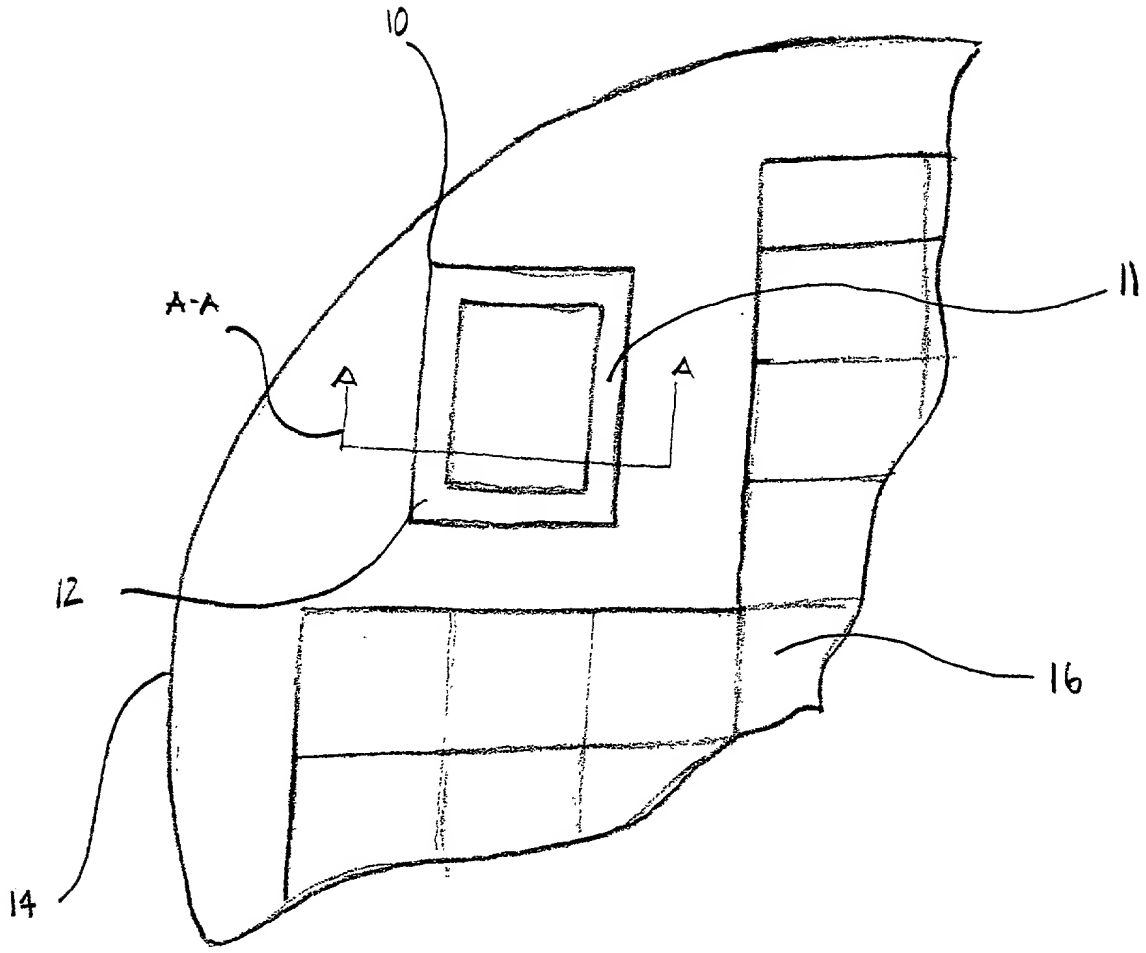

FIG. 1
(PRIOR ART)

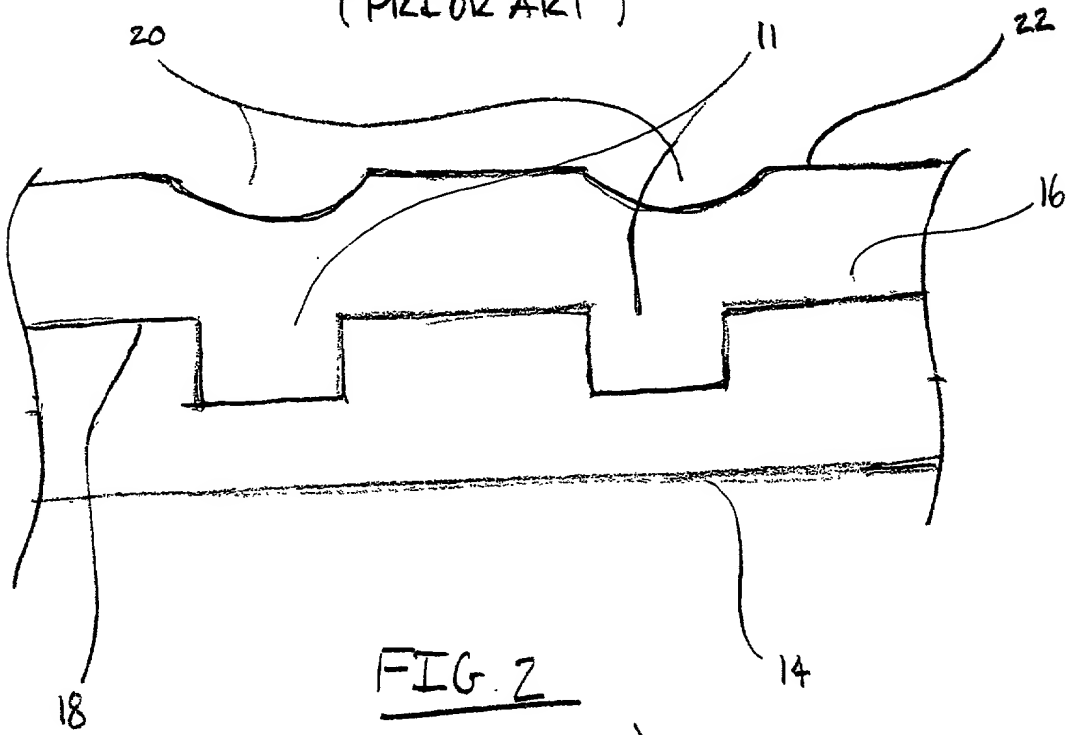

FIG. 2
(PRIOR ART)

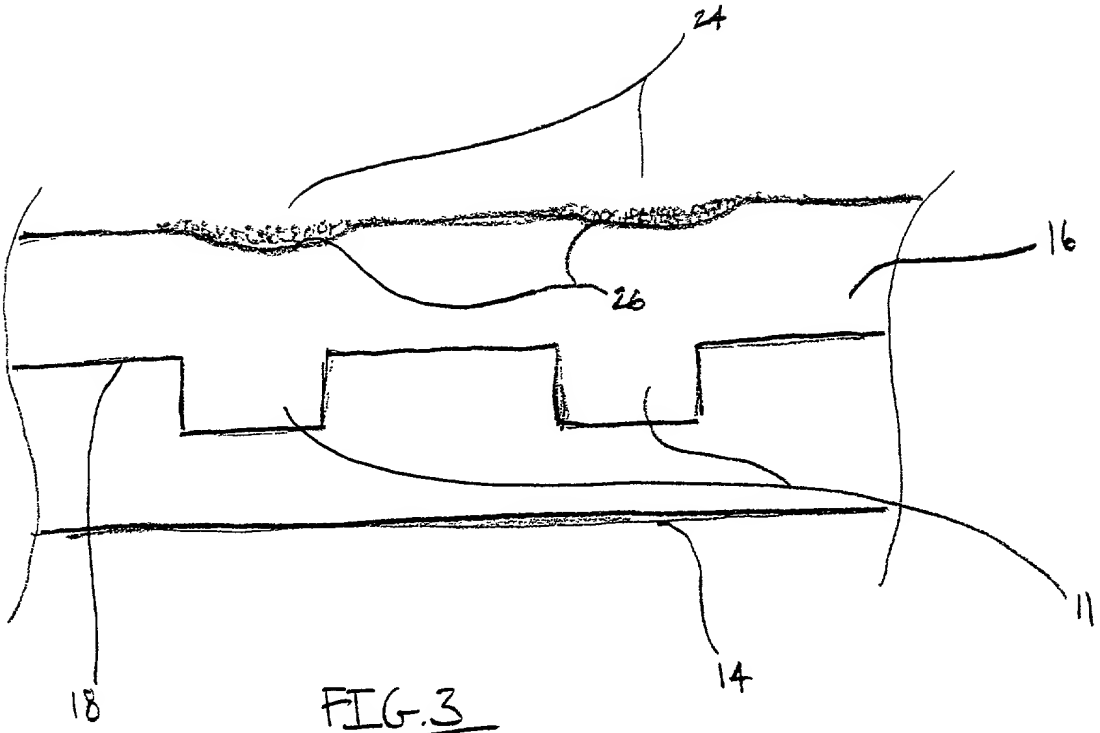

FIG. 3
(PRIOR ART)

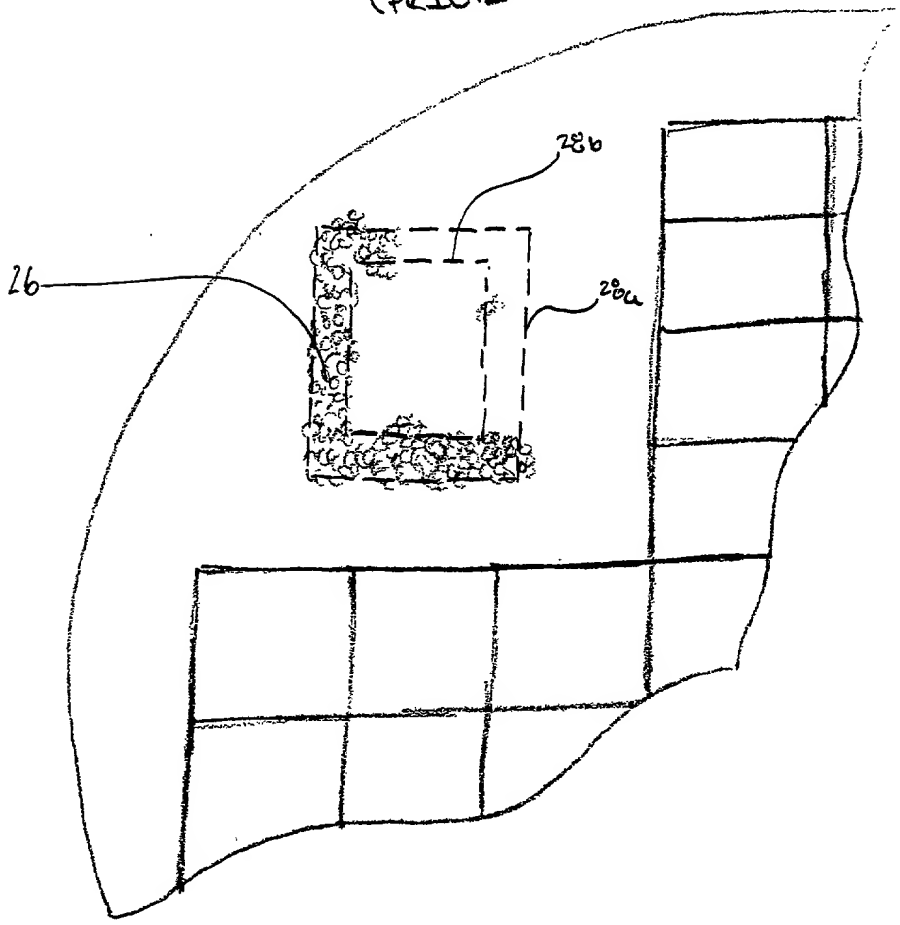

FIG. 4
(PRIOR ART)

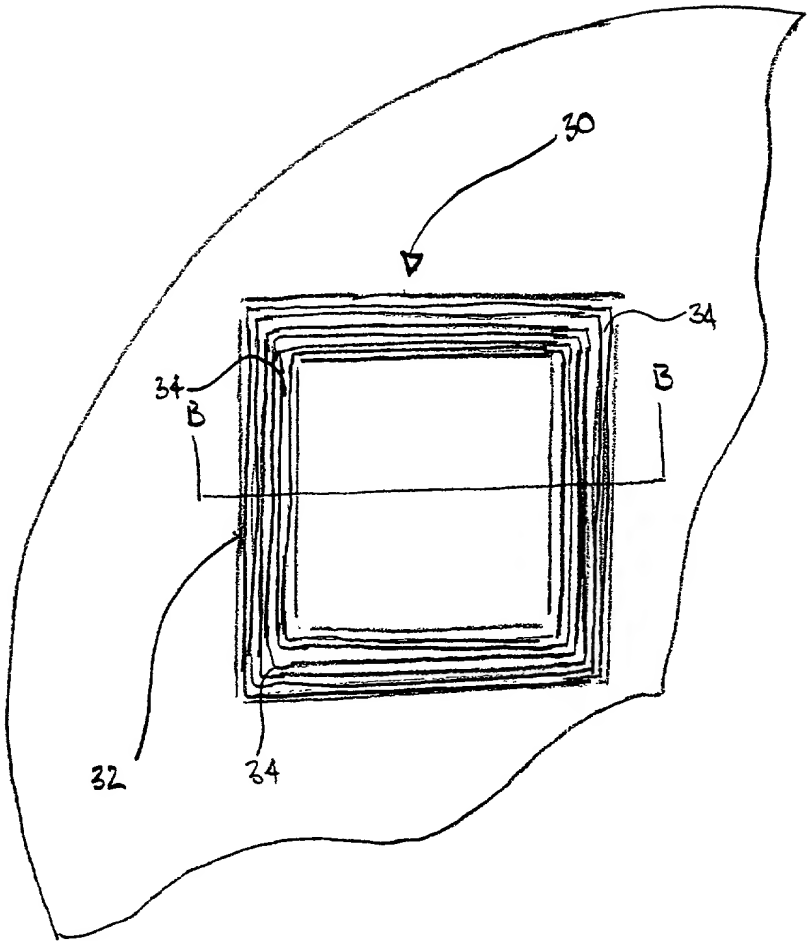

FIG. 6

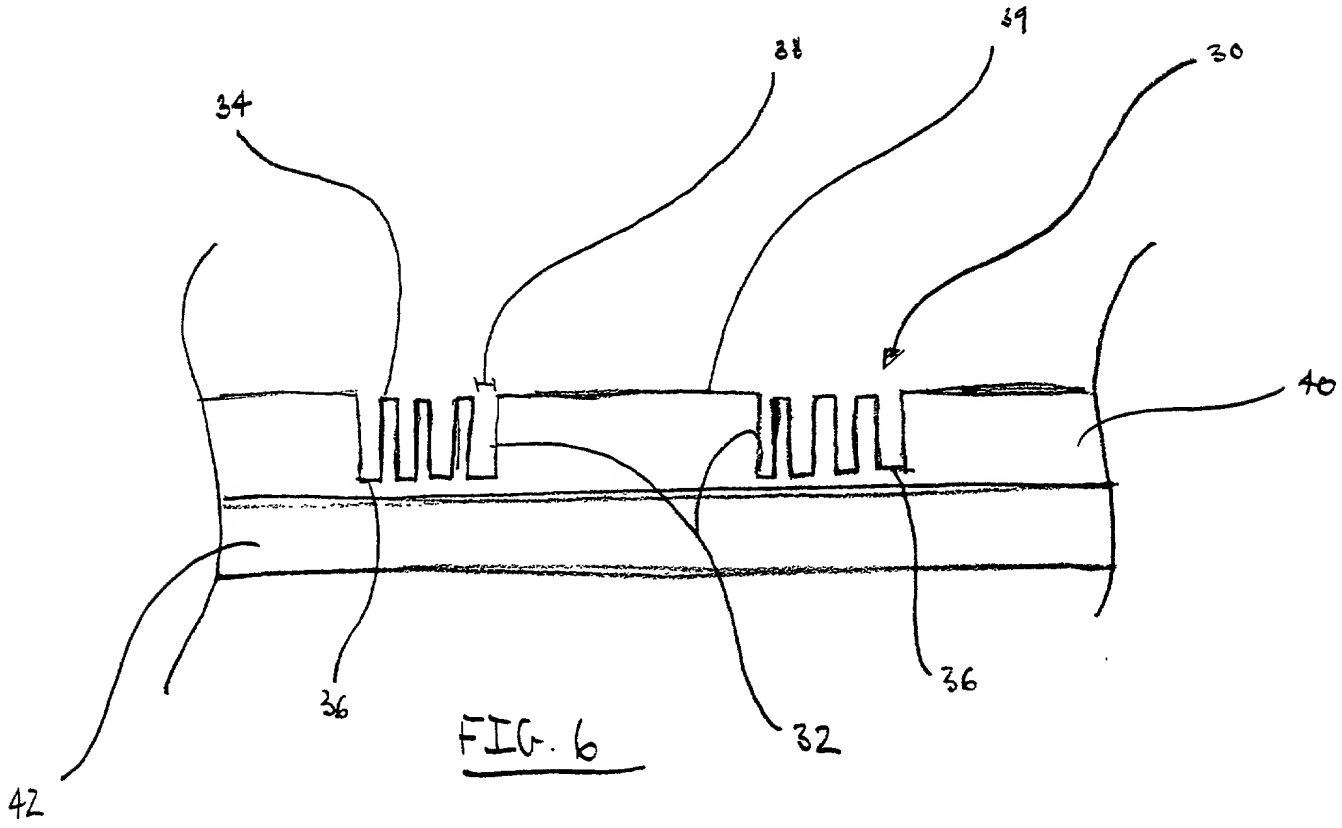

FIG. 6

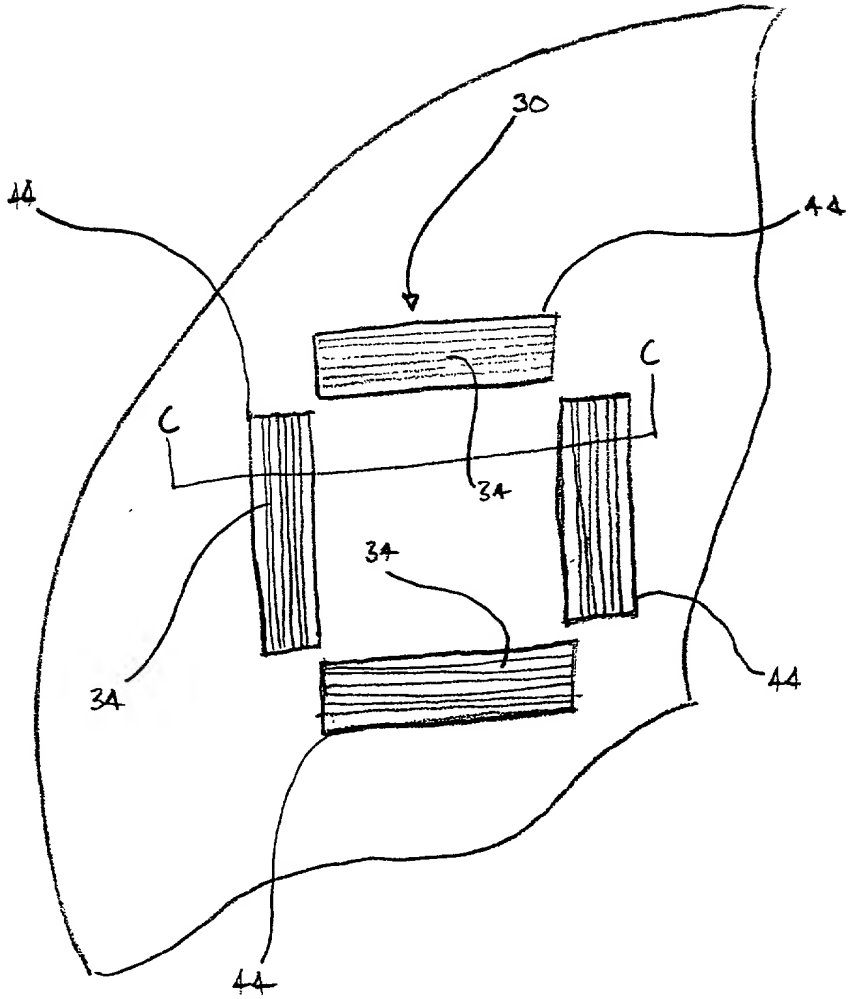

FIG. 7

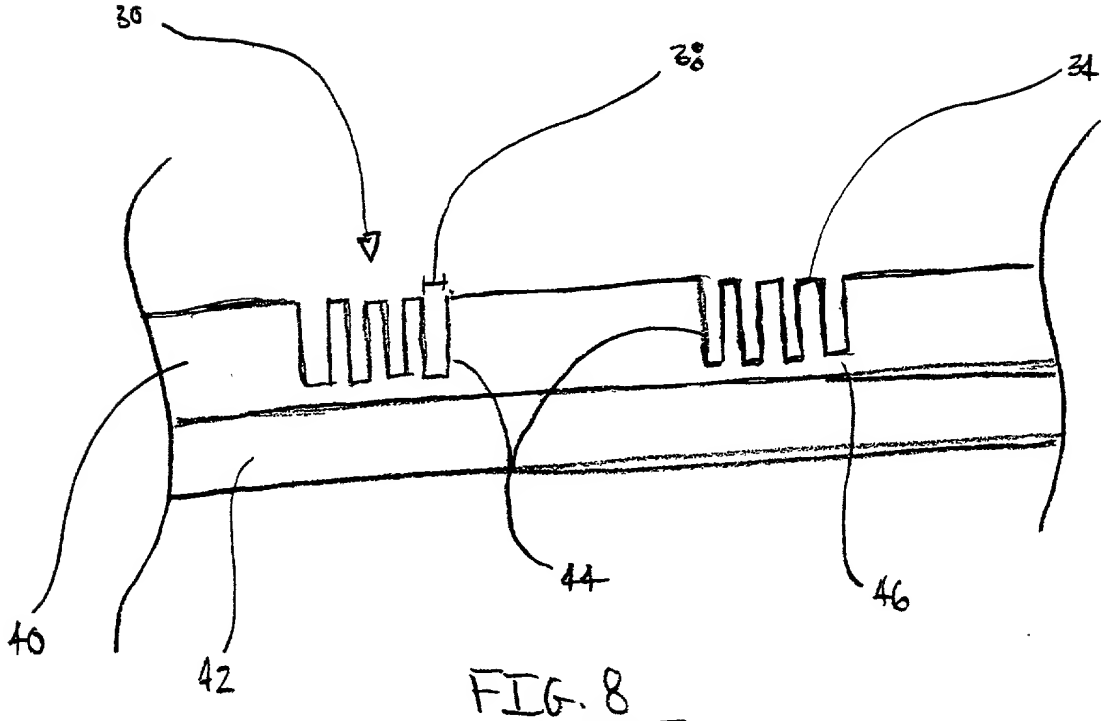

FIG. 8

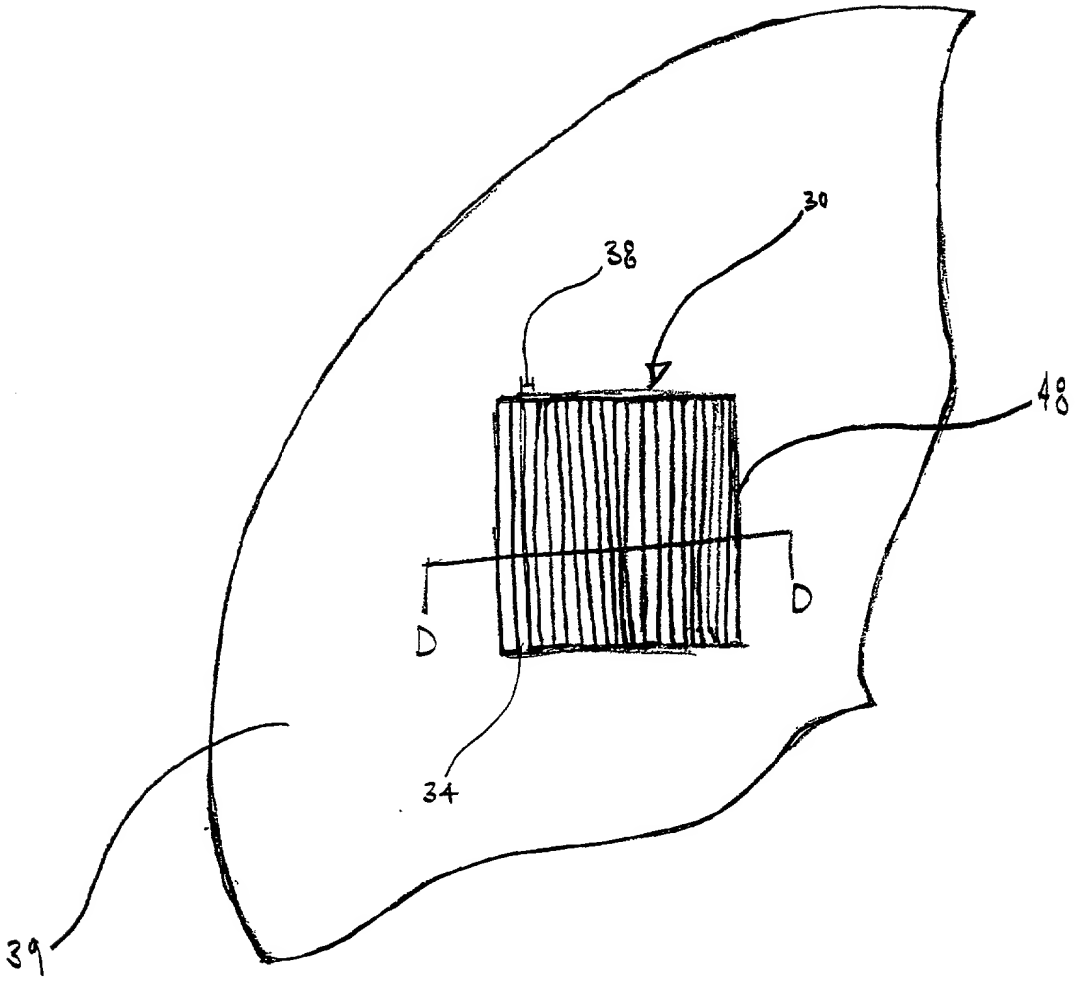

FIG. 9

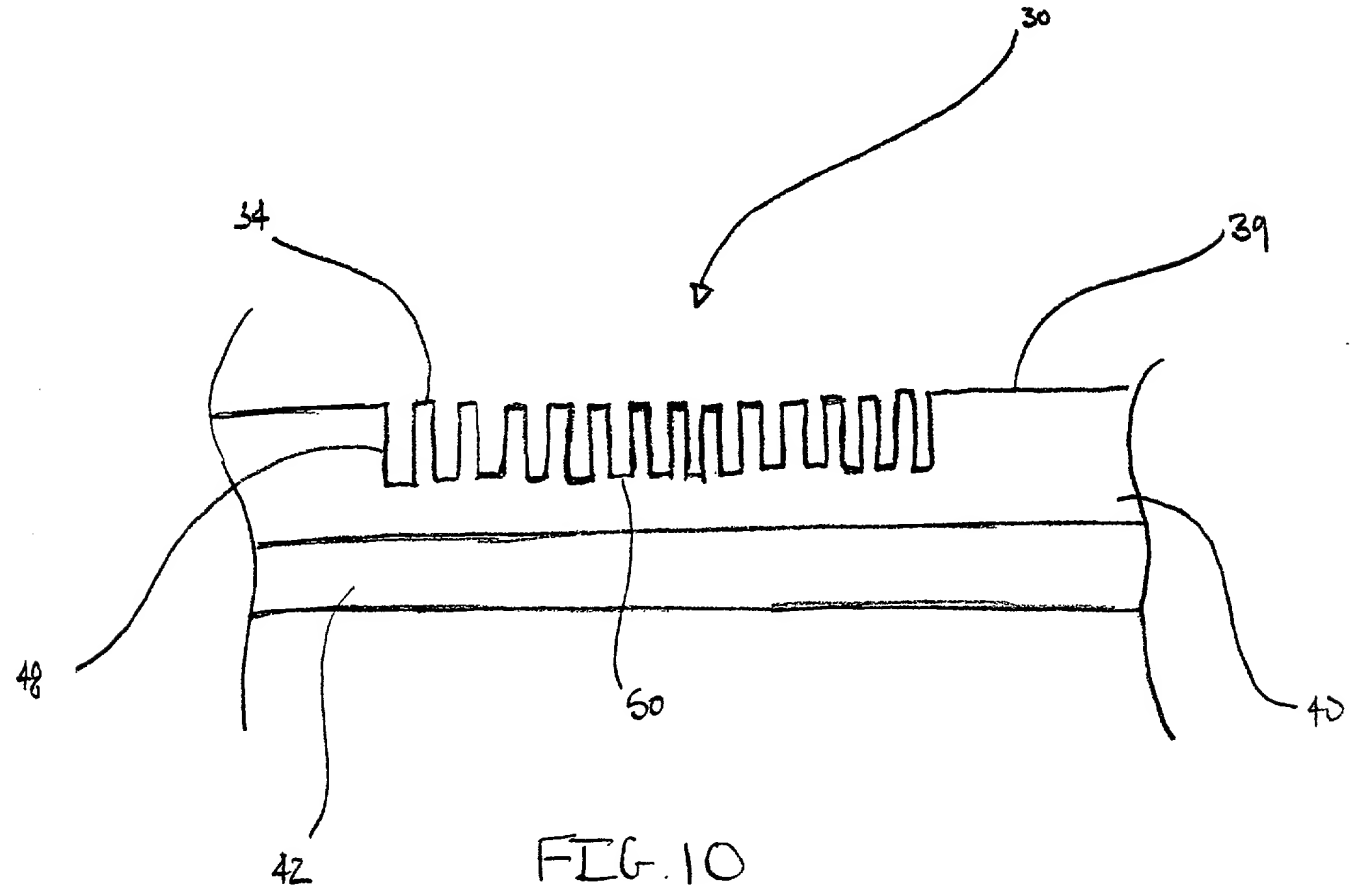

FIG. 10

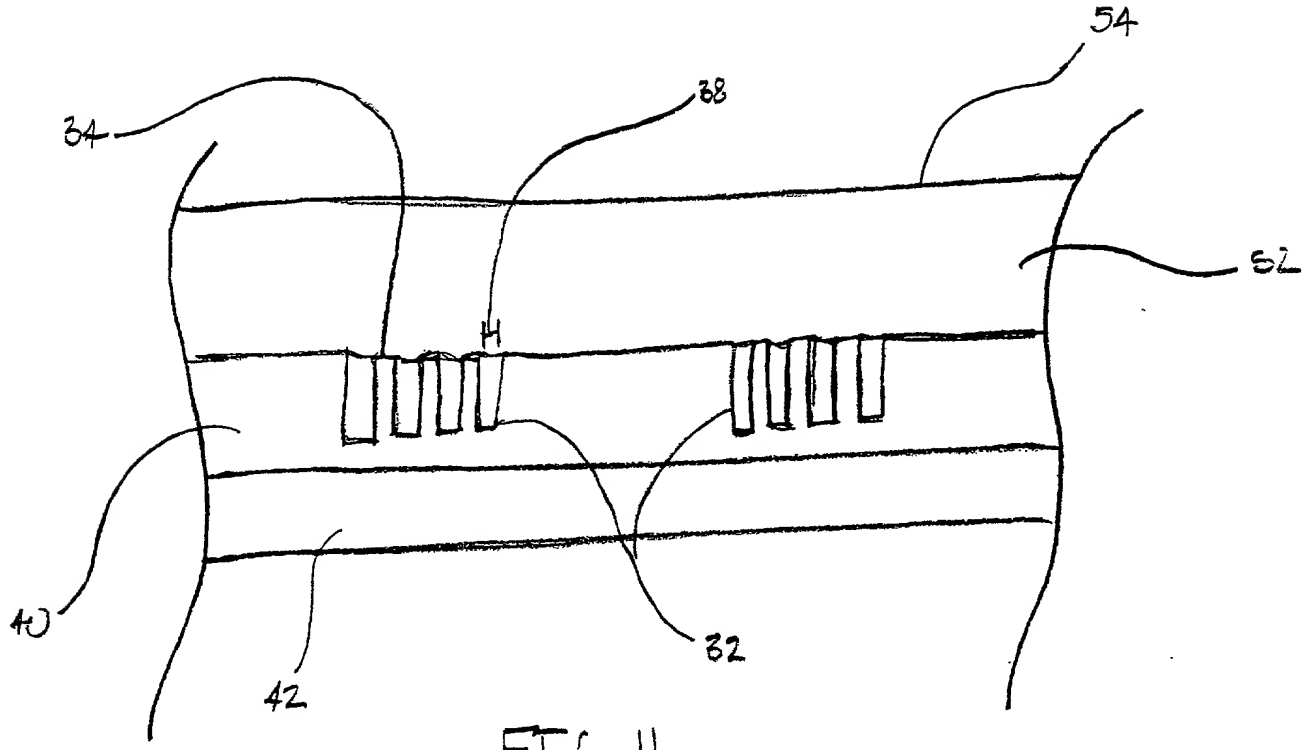

FIG. 11

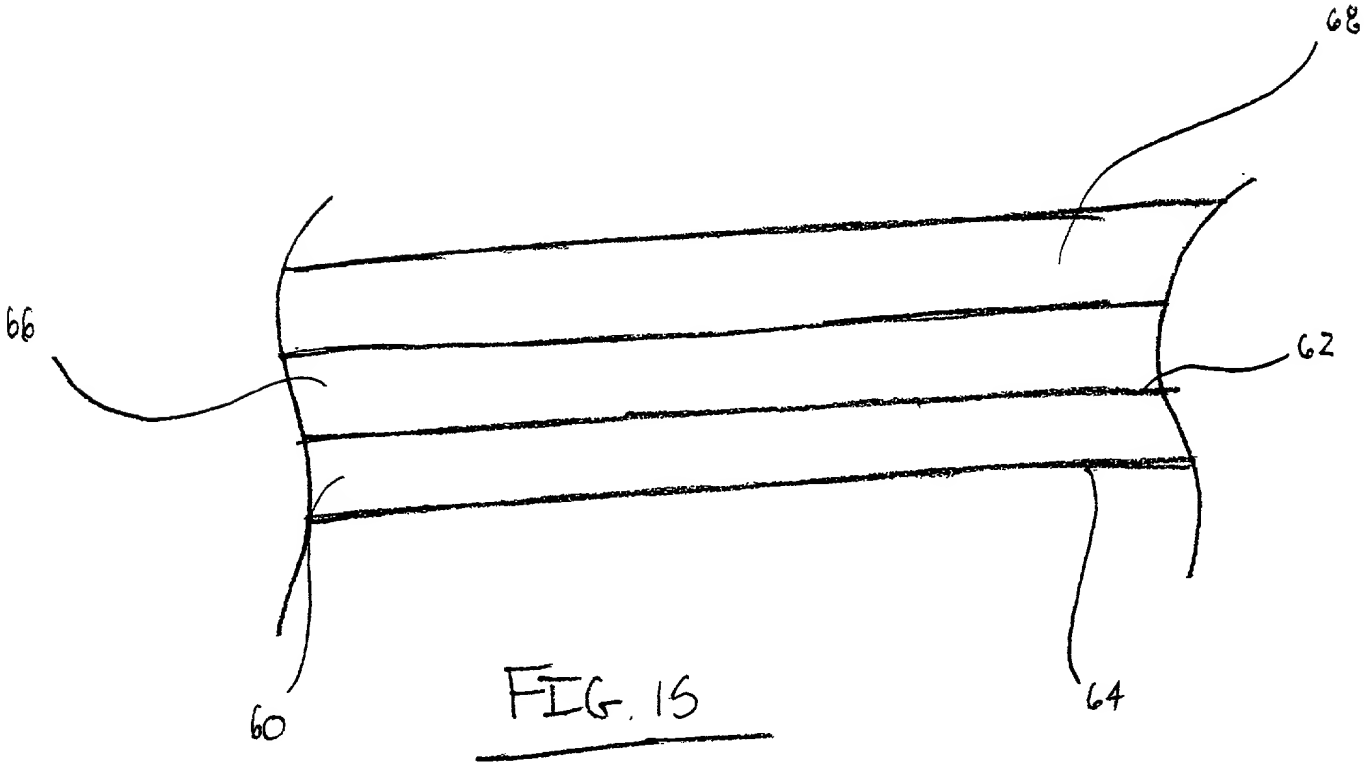

FIG. 15

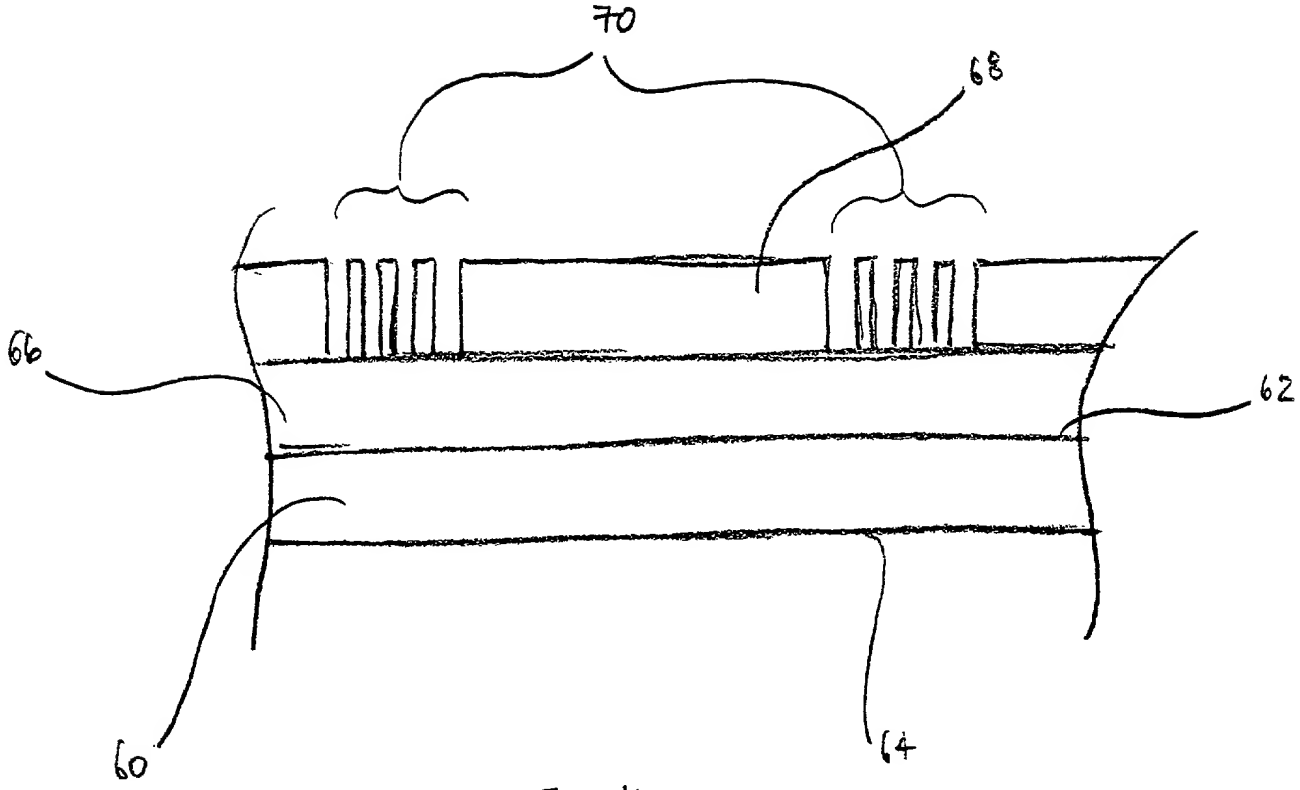

FIG. 16

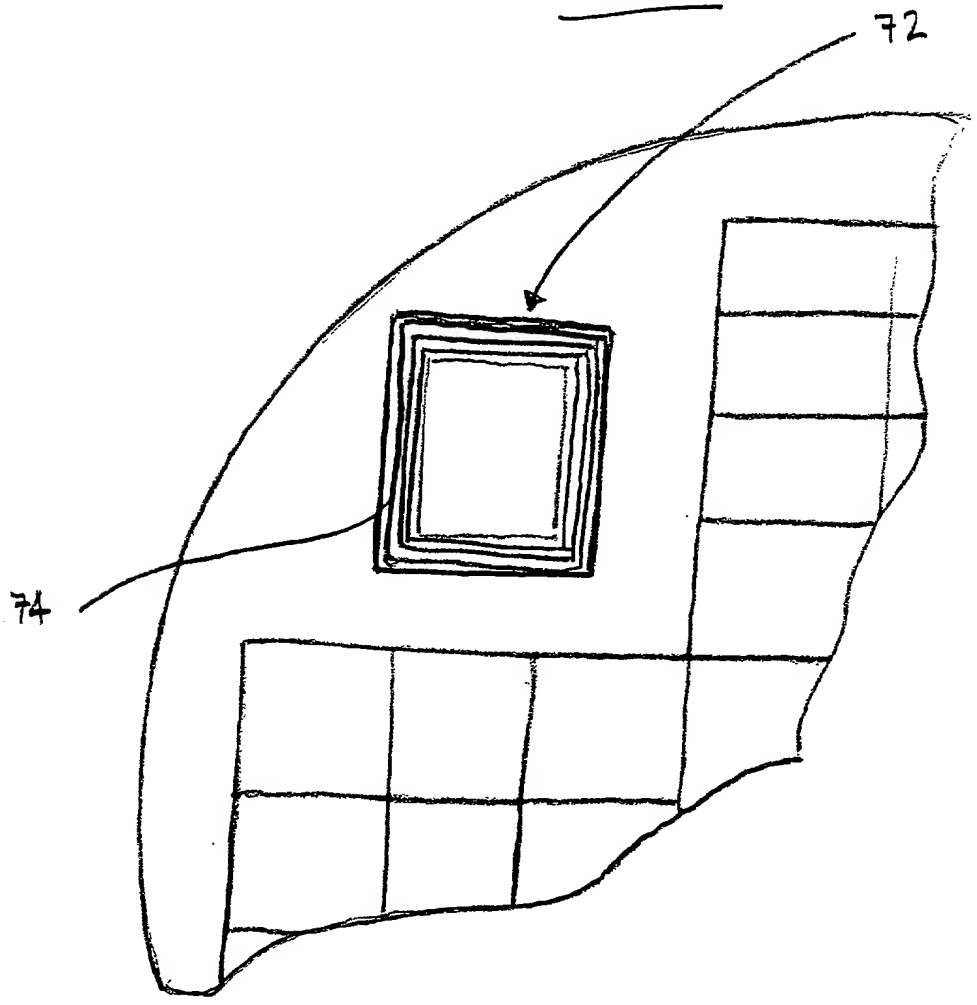

FIG. 17

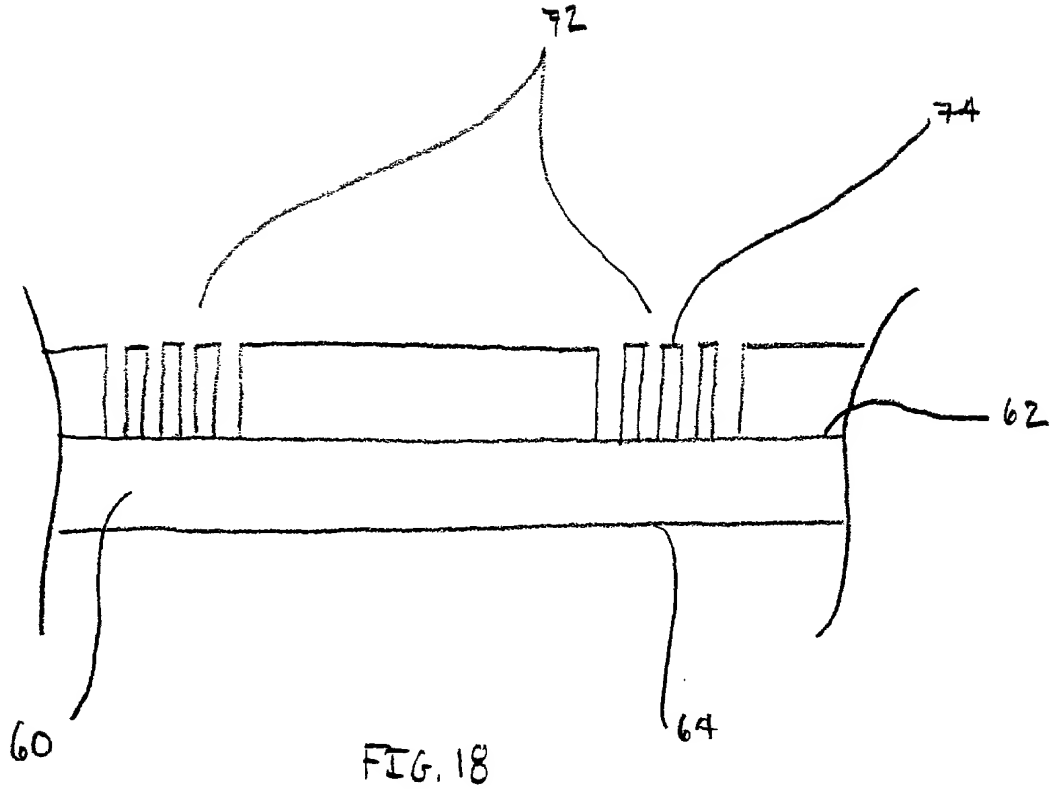

FIG. 18

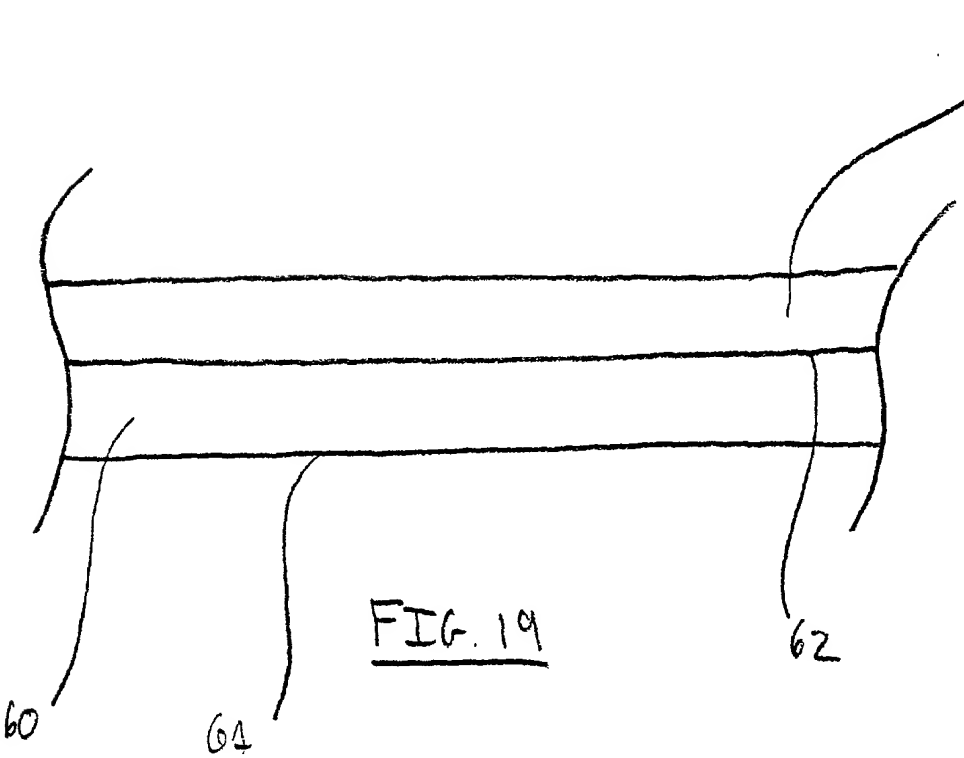

FIG. 19

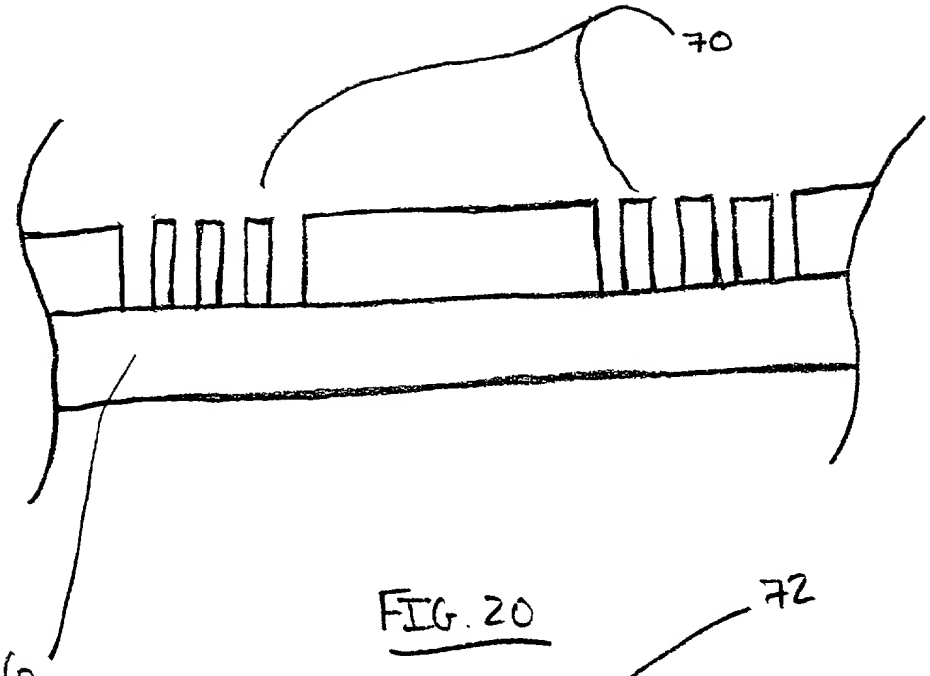

FIG. 20

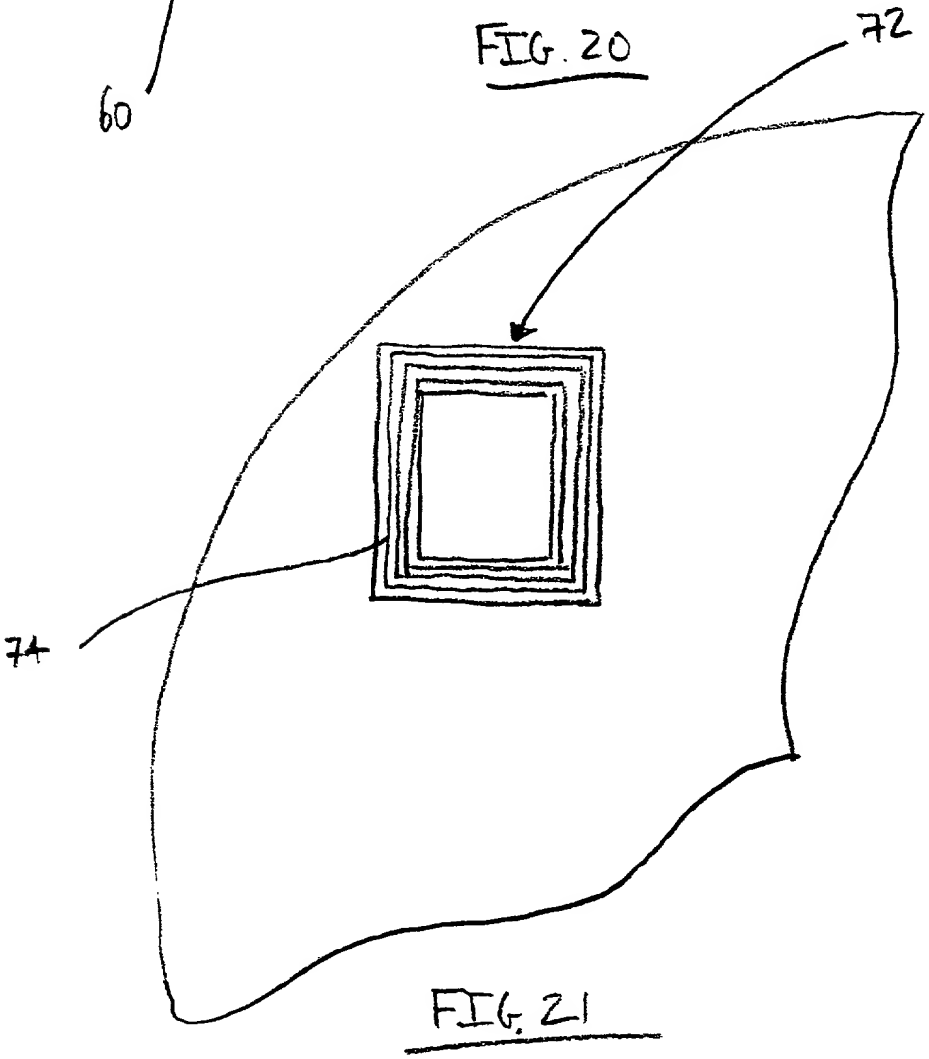

FIG. 21

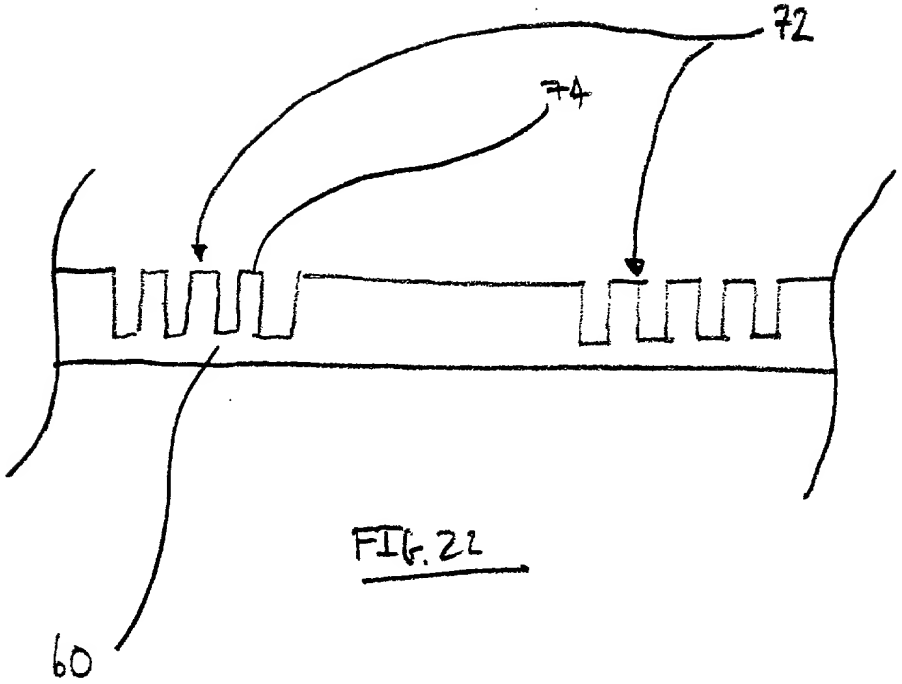

FIG. 22

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled RESIDUE FREE OVERLAY TARGET, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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TRASK BRITT
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of first joint inventor: Pary Baluswamy
Inventor's signature _____ Date _____
Residence: Boise, Idaho
Citizenship: India
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DECLARATION FOR PATENT APPLICATION
(continuation page)

Invention title: RESIDUE FREE OVERLAY TARGET

Inventor name(s) appearing on first declaration page: Pary Baluswamy

☒ Additional original, first and joint inventor(s):

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Inventor's signature _____ Date _____
Residence: Boise, Idaho
Citizenship: U.S.A.
Post Office Address: 259 East Twin Willow, Boise, ID 83706

Full name of third joint inventor: Ceredig Roberts
Inventor's signature _____ Date _____
Residence: Boise, Idaho
Citizenship: United Kingdom
Post Office Address: 1066 Hearthstone Drive, Boise, ID 83702

Full name of fourth joint inventor: Tim H. Bossart
Inventor's signature _____ Date _____
Residence: Boise, Idaho
Citizenship: U.S.A.
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